WingCore

1K/2K/4K/8K/16K/32K/40K/64K byte 1.8V EEPROM IP Macro Blocks For 0.18um CMOS Logic Process of Magnachip Product Code: WC18EH3CG, WC18EH3CW

1. General Description

"WC18EH3C" is a 2P3M (two-poly, three-metal), non-volatile EEPROM IP block which is embedded into the 0.18um standard CMOS logic process of Magnachip. As soon as a write cycle starts, the device enters into a busy state and users can easily determine whether the write cycle is completed or still under progress just by monitoring RDY signal.
Two types of versions of WC18EH3C Macro blocks are provided: WC18EH3CG and WC18EH3CW. WC18EH3CG is for "Generic process (G)" and WC18EH3CW is for "Low-power process (W)". Both types have exactly the same functionality, except stand-by current.

Table 1. WC18EH3CG and WC18EH3CW

	Condition	WC18EH3CG	WC18EH3CW
Operational Temperature	Read	-40C ~ 85C	-40C ~ 85C
	Write	-20C ~ 85C	-20C ~ 85C
Standby Current (Vcc=2V)	Typical (25C)	20uA	20uA
	Max. (85C)	100uA	50uA
Deep power-down current (Vcc=2V)	Typical (25C)	< 1uA	< 1uA
	Max. (85C)	80uA	30uA

Table 2. Page structure and Output width of WC18EH3CW

Product Code		Density	Read Speed	Page size for write	Output width for read
W-version	WC18EH3CW-1K	1Kbytes	**12MHz**	32bytes	X32
	WC18EH3CW-2K	2Kbytes			
	WC18EH3CW-4K	4Kbytes			
	WC18EH3CW-8K	8Kbytes			
	WC18EH3CW-16K	16Kbytes			
	WC18EH3CW-32K	32Kbytes		64bytes	
	WC18EH3CW-40K	40Kbytes			
	WC18EH3CW-64K	64Kbytes			

(Note 1) The output width of read is X32 (2 words)
(Note 2) WC18EH3CG has exactly the same functionality and device structure as WC18EH3CW.

2. Key Features

- 1.8V Single power supply : 1.62~1.98V
- Fast read access time: 12MHz Max.
- X32 read output, BYTEn pin don't care
- Page size (for write) : 32bytes/64bytes
- Low active current : 4mA (Typ.) at 10MHz
- Low write current: 1.5mA (Typ.)
- Write time: 8 msec/page (typical)
- Wake-up time after power-up : 100usec
- Extra user memory (XUM) : one page size for special user application
- Main functions : read, page-write, page-erase, page-program, byte-program
- Test modes : even/odd /all page-erase, even/odd/all page-program, and verify mode
- Device reset by PDOWNn pin (during power-up)
- Data retention : More than 10 years
- E/W Cycle : More than 10K

(Note) All test modes should be faithfully realized in the customer's main circuit. These modes all will be critically used for wafer-level sort later with the test time reduction. Without these modes, wafer sort and product quality can not be properly guaranteed.

Fig 1. Circuit block diagram

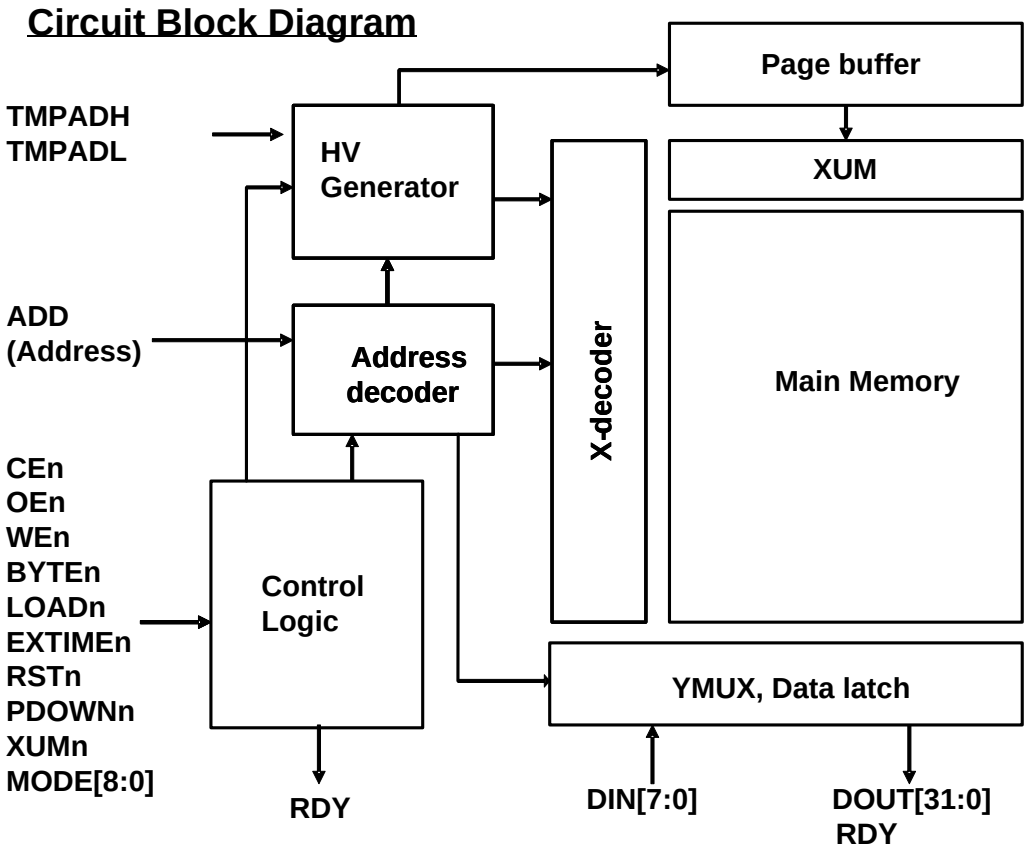


Table 3. Signal Description

Symbol	Pin name	Functions
MODE[8:5]	Test select bits	MODE[8:5] =0h for Main modes
MODE[4:0]	Mode select bits	MODE[4:0] =00h for Main modes
XUMn	Extra User Memory Enable	To write data into or read from “XUM memory” (XUMn = Low)
ADD[A_{MS}:0]	Address inputs	Memory addresses.
DIN [7:0]	Data inputs	To receive input data during write.
DOUT[31:0]	Data outputs	To output data during read.
CEn	Chip Enable	To select the EEPROM IP block.
OEn	Output Enable	“Don’t Care” Pin
WEn	Write Enable	To control write operations.
BYTEn	NC	NC
RSTn	Reset Enable	Internal registers or latches including the page-buffer are all reset by RSTn signal. Any operation under progress is immediately terminated by the device reset.
LOADn	Load Enable	To load data into page-buffer for a write operation
RDY	Ready	To determine when a write operation is completed. RDY=high for “ready to read”, low for “busy during write operation”.
PDOWNn	Power-down mode Enable	“ PDOWNn at low” forces the IP block to enter “deep power-down mode”. In this mode, the current consumption is deeply suppressed down to 1uA, typically. And, this PDOWNn signal should be kept at low during power-up for safe initialization
EXTIMEn	External Time Enable	This signal is used for two purposes. 1) Synchronous Clock signal for read operation as a sort of ATD (Address transition pulse) 2) To externally and freely control the period of erase or program time by forcing EXTIMEn to low.

Note) A_{MS} : The Most Significant Address Bit

3. Functional Modes

There are two groups of functional modes: **Read modes** and **Write Modes**. One of the functions can be freely selected by **Mode bits [4:0]** as shown in the table 4.

- All erase operations are performed by a page unit, not a byte.
- All program operations are also performed by a page unit.
- A specific cycle called "**LOAD**" should be first executed to load data into an internal page-buffer before any write operation starts.
- Basically, a page-erase or a page-program is separately performed..
- But, a page-write operation is internally composed of two operations. A page-erase is first performed and then a page-write is automatically followed.
- At least, one byte should be loaded into the page-buffer to activate any following write operations like a page-write, a page-program, including **even a page-erase**
- In a page-erase, all the bytes in the selected page are completely erased regardless of the content of the page-buffer. However, it should be noted that a byte at minimum should be loaded to activate the erase operation.
- In a page-program or a page-write, one or any number of bytes (limited to the given page size) can be loaded into the page-buffer. In other word, one-byte program is allowed if just one-byte is loaded. But, you should remember that all bytes (the previously written data) of a selected page are completely erased before one-byte is programmed even if only one-byte is loaded at the page-write function.

Table 4. Functions and Mode selection bits (MODE[4:0])

Mode	Functions		MODE [4:0]
Read Mode	Reset		00h
	Deep Power-down		
	Standby		
	Read		
	Verify	Erase-verify	14h
		Program-verify	18h
Write Mode	Write	Single page-write	00h
		All Page-write	03h
	Erase	Single page-erase	04h
		Even page-erase	05h
		Odd page-erase	06h
		All page-erase	07h
	Program	Single page-program	08h
		Even page-program	09h
		Odd page-program	0Ah
		All page-program	0Bh

Table 5. Pin description and status

	Modes						
	Reset	Deep power-down	Standby	Read	Page-Write		
				X32	Load	page Erase	page Program
MODE[4:0]	x	x	x	00	00	00	00
XUMn	x	x	x	H	H	H	H
BYTEn	x	x	x	x	x	x	x
ADD [byte]	x	x	x	Ain	Ain	x	x
ADD [page]	x	x	x	Ain	Ain	Ain	Ain
Din[7:0]	x	x	x	x	Din	x	x
DOUT[31:0]	x	x	x	Dout	x	x	x
CEn	x	x	H	L	L	L	L
OEn	x	x	x	x	x	x	x
WEn	x	x	x	H	L	H	H
LOADn	x	x	x	H	L	H	H
RSTn	L	x	H	H	H	H	H
PDOWNn	H	L	H	H	H	H	H
EXTIMEn	x	x	x	Toggle	Toggle	H	H
RDY	H	H	H	H	H	L	L

(Note) Hi-Z : High-impedance state, x : Vil or Vih for input, Vol or Voh for output
ADD[1:0] are don't care in read mode.

Caution

1. "Byte by byte" operation is not allowed for erase operations.
   -Write
   -Erase
2. Only "page operation" is allowed for erase operations.

4. Read Mode

PDOWNn should be kept at low during power-up to correctly initialize the device. But at least 100usec of wake-up time after power-up is required to perform any normal operation like Read. After 100usec of wake-up time, the device automatically enters the read mode..
Chip Enable (CEn) is used for the device selection. As shown in Fig. 2, **400nsec** of the wait-time (tCES) is required before the first read is performed.
After the device enters the read-mode, any valid address can be sequentially asserted while "EXTIMEn" signal toggles. A read data is sensed while EXTIMEn stays at low for 40nsec (tEXTL). And then the sensed data is latched at a little time after the rising edge of EXTIMEn. The valid data output gets available at output nodes, tVFA later from the rising edge of EXTIMEn. EXTIMEn operates as a clock for synchronous read operation.
Here, it should be noted that address is not latched in read operation. So, valid address needs to be kept stable during read operation.

Fig 2. Read Operation Timing Diagram

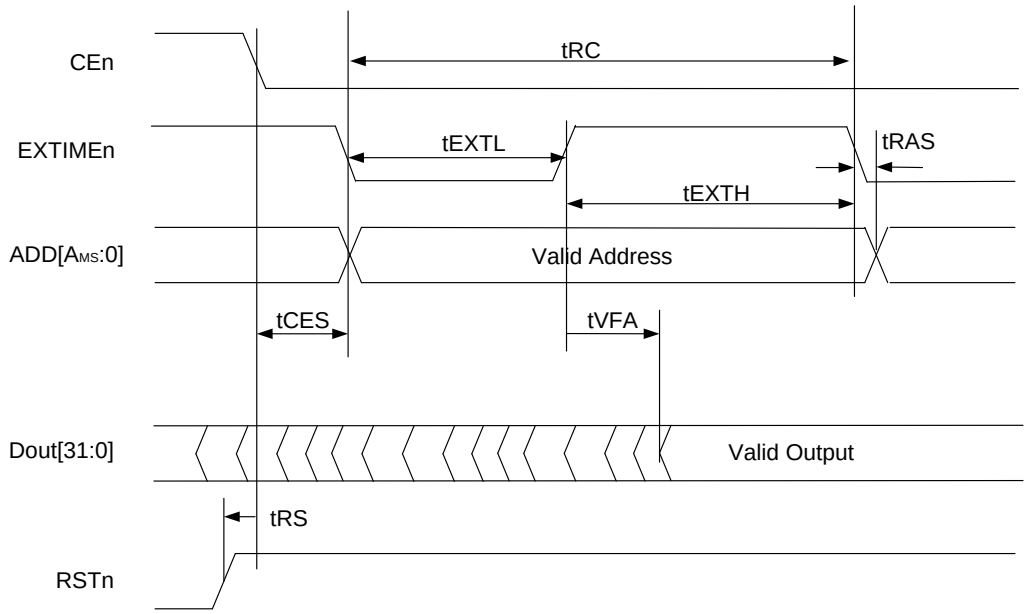


Table 6.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRC	Read Cycle Time	83			ns
tCES	CEn Setup time	**400**			ns
tEXTL	EXTIMEn Low Width	40			ns
tEXTH	EXTIMEn High Width	40			ns
tRAS	Address Setup time	0			ns
tVFA	EXTIMEn to Output Valid			35	ns
tRS	RSTn Setup Time	100			ns

Note) Cload [Load Capacitance at output node] is assumed to be less than 0.3pF.

5. Verify Mode

Two verify-modes are supported: **erase-verify** and **program-verify**. They are a sort of special read mode, but their internal operations are much different from the normal read which simply gets out data which was stored in the memory array. This verify operation can be used usefully, combined with either erase or program operation. By using these verify-modes, any byte in the memory can be selected and checked for how much programmed or erased they are and the results can be easily read out to outputs just like the normal read operation. Some reference levels respectively for programmed or erased bits are internally set in the device. Therefore, correct results can be read out to the outputs, only when the selected bits (or bytes) are programmed or erased enough exceeding the internal reference levels. Therefore, these verify-modes are frequently and critically used for the wafer-level sort.

The erase-verify and the program-verify mode is respectively activated by 14h and 18h of MODE [4:0] defined in the table 4. As shown in Fig. 3, **50usec** of the wait-time (tVFD) is needed after CEn is driven to low before the verify-operations are ready.
After the device enters the verify-mode, any valid address can be sequentially asserted while “EXTIMEn” signal toggles. Data is sensed while EXTIMEn stays at low for 40nsec (tEXTL). And then the verified (or sensed) value is latched, a little time later after the rising edge of EXTIMEn. The valid data (verified result) gets available at output nodes, tVFA later from the rising edge of EXTIMEn.

Fig. 3 Verify timing diagram

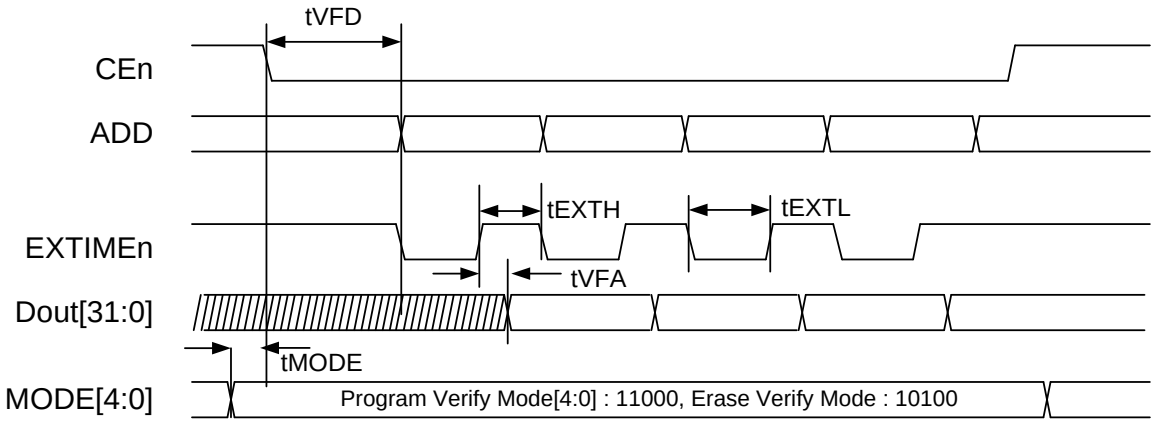


Table 7.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tVFD	Verify Dummy Time	**50**			us
tEXTL	EXTIMEn Pulse Low Width	40			ns
tVFA	EXTIMEn to Valid Output Time			35	ns
tMODE	MODE pin Setup Time	0			ns
tEXTH	EXTIMEn Pulse High Width	40			ns

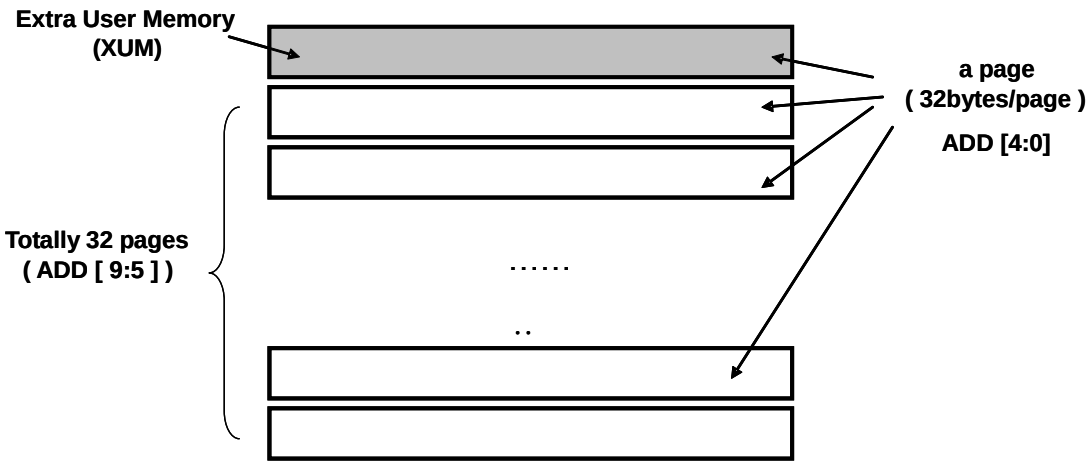
6. Page-Write

The write operation is executed, based on “page by page.” For writing actual data into the memory array, data should be first loaded into an internal **page-buffer** through data load cycle (LOAD). A page is composed of 32bytes or 64bytes depending on the memory density of the device the whole memory array is composed of multiple pages. Refer to table 8 and Fig. 4 to see how pages are organized into the whole memory array.

Table 8. Page and Byte addresses for each IP block with different memory density

Product code	Memory size		Page size	Byte address	Page address
	Bytes	bits			
WC18EH3CG/W-1K	1K bytes	8Kbits	32bytes	ADD[4:0]	ADD[09:5]
WC18EH3CG/W-2K	2K bytes	16Kbits			ADD[10:5]
WC18EH3CG/W-4K	4K bytes	32Kbits			ADD[11:5]
WC18EH3CG/W-8K	8K bytes	64Kbits			ADD[12:5]
WC18EH3CG/W-16K	16K bytes	128Kbits			ADD[13:5]
WC18EH3CG/W-32K	32K bytes	256Kbits	64bytes	ADD[5:0]	ADD[14:6]
WC18EH3CG/W-40K	40K bytes	320Kbits			ADD[15:6]
WC18EH3CG/W-64K	64K bytes	512Kbits			ADD[15:6]

Fig. 4 Physical organization of bytes and pages (1Kbytes Macro block for an example)



Actually, the page-write operation is composed of three separate operations: Load, Page-erase and Page-program. As shown in the Fig.6, data should be first written into the page buffer while LOADn is kept at low. Once after LOADn is driven to High from Low, **RDY** signal automatically goes to low, indicating that the write operation is started and under progress.

Typically 8 msec of write time (tWRITE) is internally assigned, so tWRITE can not be changed or controlled by users.

A load operation is automatically followed by a page-erase and a page-program operation once after data is loaded into the page buffer. Here, “0” data means “an erased bit”, while “1” data means “a programmed bit”. It should be noted that “1” can not be programmed back into “0” by the program operation, while “1” can be changed to “0” only by erase operation. Refer to Fig.6 for write timing.

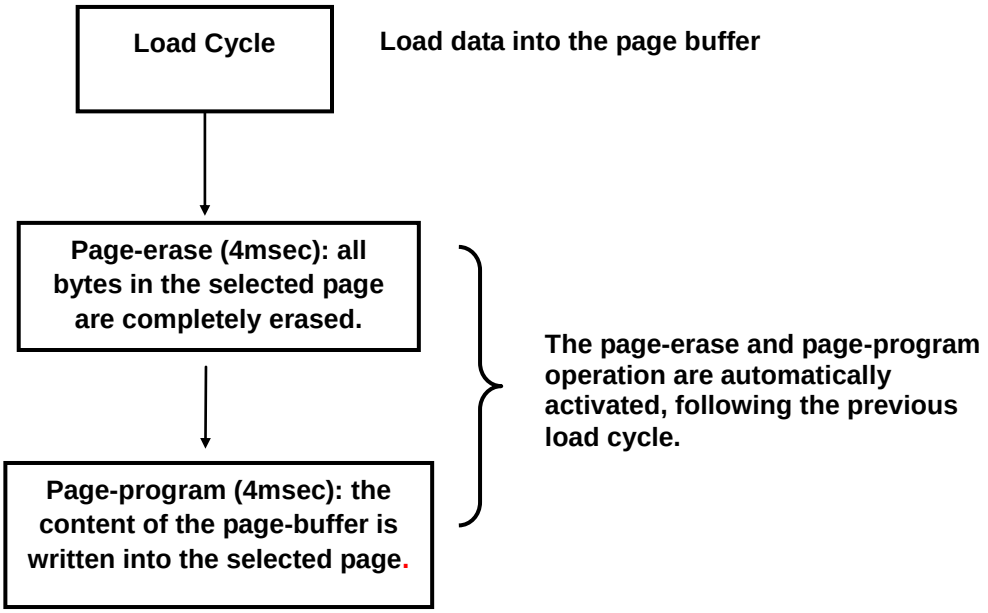


Fig. 5 Page-Write Operation

RDY, a status bit for Write Operation

“RDY signal” is a status bit for write operation, including page-erase or page-program.
This signal can be used to check or monitor when the write operation actually starts or is completed. **“**Data load into the page-buffer” is terminated by driving “LOADn” from Low to High. Then, “actual write operation” starts tBUSY later after LOADn goes to High. At the same time, “RDY” goes to Low to indicate that “write operation is under progress. The write operation (erase + program) is executed for typically 8msec (tWRITE). As soon as the write operation is completed, RDY goes from Low to High. During the whole write operation, the page and byte address should be kept stable, as shown in the Fig.6.

CEn toggle between different operations

When CEn goes from low to high, the device is all reset, including “page-buffer”. So, “CEn toggle” needs to be properly inserted before moving to another operation from the current write operation. If the page-buffer is not properly cleared (reset), unexpected result can happen in the next write operation. Refer to “tCEH and tRHCH” in Fig.6.

Fig 6. Write Operation Timing Diagram

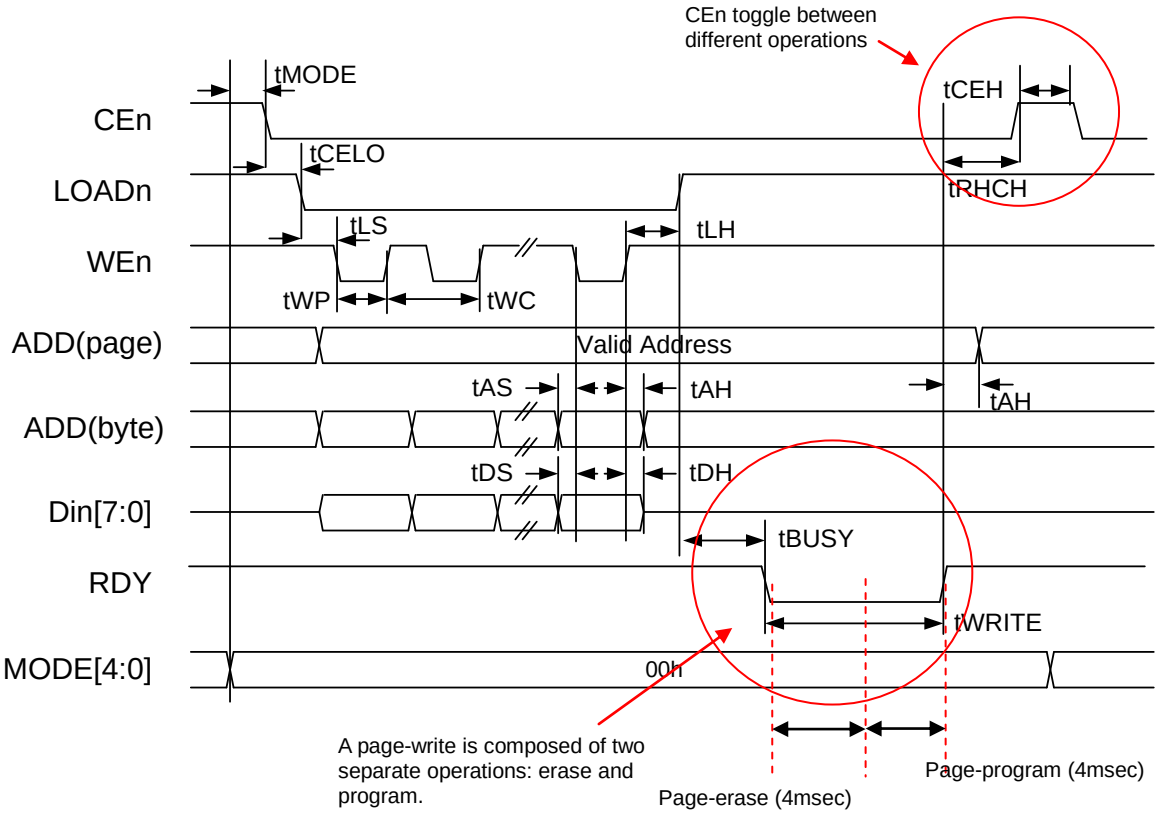


Table 9.

Symbol	Parameter		Min.	Typ.	Max.	Unit
tWC	Write Cycle Time		50			ns
tWP	Write Pulse Width		20			ns
tAS	Address Setup Time		5			ns
tAH	Address Hold Time		5			ns
tDS	Data Input Setup time		5			ns
tDH	Data Input Hold time		5			ns
tMODE	MODE pin Setup Time		0			ns
tCELO	CEn Low to LOADn Low time		0			ns
tRHCH	RDY High to CEn High time		0			ns
tCEH	CEn High Width		20			ns
tLS	LOADn Setup Time		50			ns
tLH	LOADn Hold Time		50			ns
tBUSY	RDY "low" Delay Time		200			ns
tWRITE	page-write time	Total time	6	8	10	ms
		Page-erase	3	4	5	ms
		Byte or page-program	3	4	5	ms

Note) If "RDY" signal is not used, maximum time should be assigned for page-write operation, considering the process variation.

7. Data Load

Data should be first loaded into the page-buffer before any actual write operations start. Initially, the page buffer is reset to all "0 (erased bit)" after power-up or can be intentionally reset to all "0" by RSTn. Any number of bytes can be loaded in any order the maximum number of bytes that is equal to a specific page-buffer size (Table8 for page sizes). The byte-data are respectively selected (or identified) by their byte addresses. However, the specific "page address" should be kept stable for the period in which bytes data are loaded and the following erase and program operations are executed. This stability of the page address is required to guarantee correct data to be written into the actual memory array. If not, data will be written into an unwanted or incorrect page location.

During data load operation, data is latched at the high edge of WEn while address is not latched.
However, "data change" is not allowed anyhow during the low period of WEn before the data is finally latched. Any data change may affect the final result latched at the rising edge of WEn.
Therefore, to load the correct data, byte-addresses and data should be kept stable (should not be changed) during the whole low period of WEn. (Refer to Fig.6)

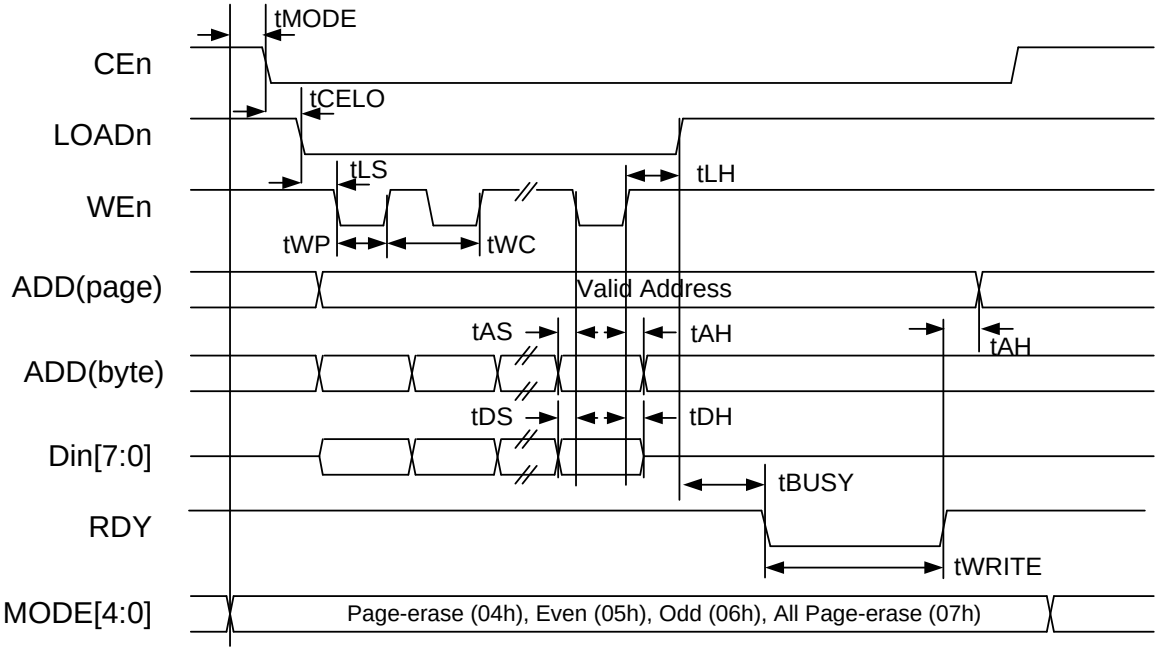
8. Erase Modes

One of the four erase-modes can be selected by MODE[4:0] as shown in the table 10 below. Each erase-mode is functionally the same as the others. They can be all separately operated, but one byte at minimum should be loaded into the page-buffer for any type of erase modes.
However, it should be noted that “byte-based erase” is not allowed. Only “page-based erase” is supported.

Table 10.

Type	Modes	Eased pages	MODE [4:0]
Erase modes	**Single page-erase**	Only a selected single page is completely erased.	**04h**
	Even page-erase	All even pages in the whole memory are erased at once.	**05h**
	Odd page-erase	All odd pages in the whole memory are erased at once	**06h**
	All page-erase	All pages in the whole memory space are erased at once	**07h**

Fig. 7 Timing diagram for the erase-modes



9. Program Modes

Table 11.

Type	Modes	Programmed pages	MODE [4:0]
Program Mode	Single page program	Only a selected single page is programmed.	**08h**
	Even page-program	All even pages in the whole memory are programmed with the same pattern (which is previously loaded into the page-buffer)	**09h**
	Odd page-program	All even pages in the whole memory are programmed with the same pattern	**0Ah**
	All page-program	All pages in the whole memory are programmed with the same pattern	**0Bh**

10. How to effectively generate “CKB (Checker Board) pattern”

1. Load a byte to the page-buffer
2. All page-erase
3. Load “AA55” repeatedly into the page-buffer
4. Even page-program
5. Clear the page-buffer by “device reset”.
6. Load “55AA” repeatedly into the page-buffer
7. Odd page-program

11. User-Time Controlled Write (EXTIMEn)

In the normal write mode, the period of the total write time (including the page-erase and page-program) is internally fixed to 8msec, which is not allowed to be changed by users. But, in the user-time controlled write mode driven by EXTIMEn signal, erase or program time can separately controlled by users, just by increasing or decreasing the low duration of EXTIMEn as shown in Fig 8. However, this “user-time controlled write” should be only applied to the additional erase or program-modes defined in the table 12. This “user-time controlled write” is not recommended for the main page-write in which both the erase and program operation are included. But, this special write mode may be very useful especially when it is used for some special user purposes, like product test, verification, and enhancing the reliability in some cases.

After the user-time controlled write is terminated by driving EXTIMEn to high from low, at least **20us of recovery time** (**tREADY**) is required to get out of the internal high-voltage write operations to return to the normal read mode.

Fig 8. Timing diagram of user-time controlled write by EXTIMEn

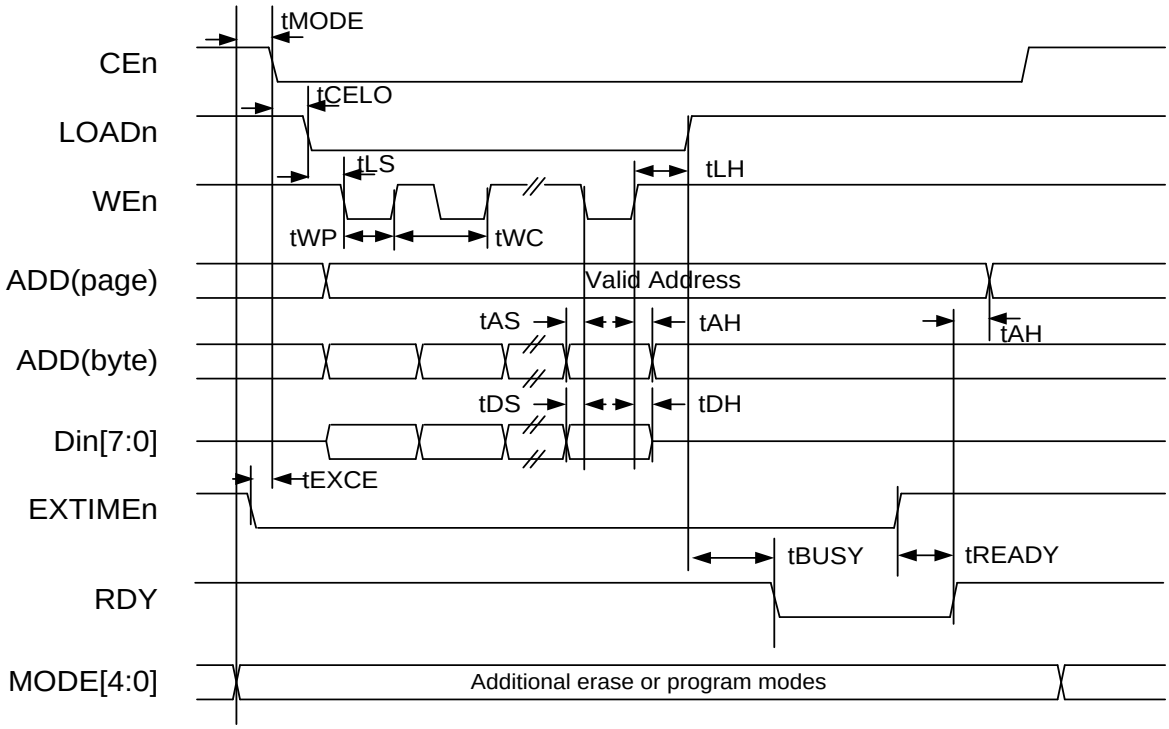


Table 12

Symbol	Parameter	Min.	Typ.	Max.	Unit
tWC	Write Cycle Time	50			ns
tWP	Write Pulse Width	20			ns
tAS	Address Setup Time	5			ns
tAH	Address Hold Time	5			ns
tDS	Data Input Setup time	5			ns
tDH	Data Input Hold time	5			ns
tMODE	MODE pin Setup Time	0			ns
tCELO	CEn Low to LOADn Low time	0			ns
tLS	LOADn Setup Time	50			ns
tLH	LOADn Hold Time	50			ns
tBUSY	RDY “low” Delay Time	200			ns
tREADY	RDY “high” Delay Time			20	us
tEXCE	EXTIMEn Setup Time		0		ns

12. Extra User Memory (XUM)

One page size of extra memory called XUM is provided for users’ specific purposes like storing test codes, product code, or some security serial numbers. The extra memory is selected only when XUMn is at low.

Table 13

		XUMn=high		XUMn=low	
Mode	Functions	Main	Extra	Main	Extra
Normal	Read	●	X	X	●
	Page write	●	X	X	●
Erase	Single page-erase	●	X	X	●
	Even page-erase	●	X	X	●
	Odd page-erase	●	X	●	●
	All page-erase	●	X	●	●
Program	Single page-program	●	X	X	●
	Even page-program	●	X	X	●
	Odd page-program	●	X	●	●
	All page-program	●	X	●	●

Fig. 9 Timing diagram of XUM

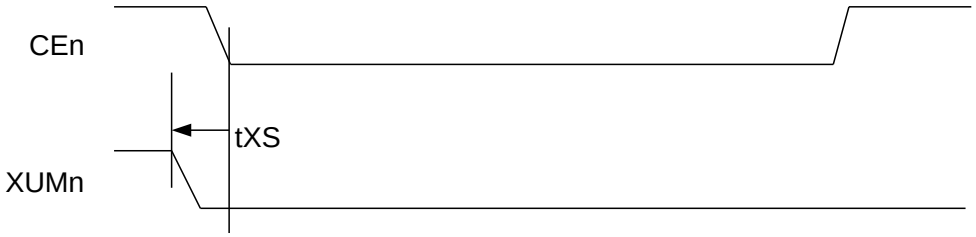


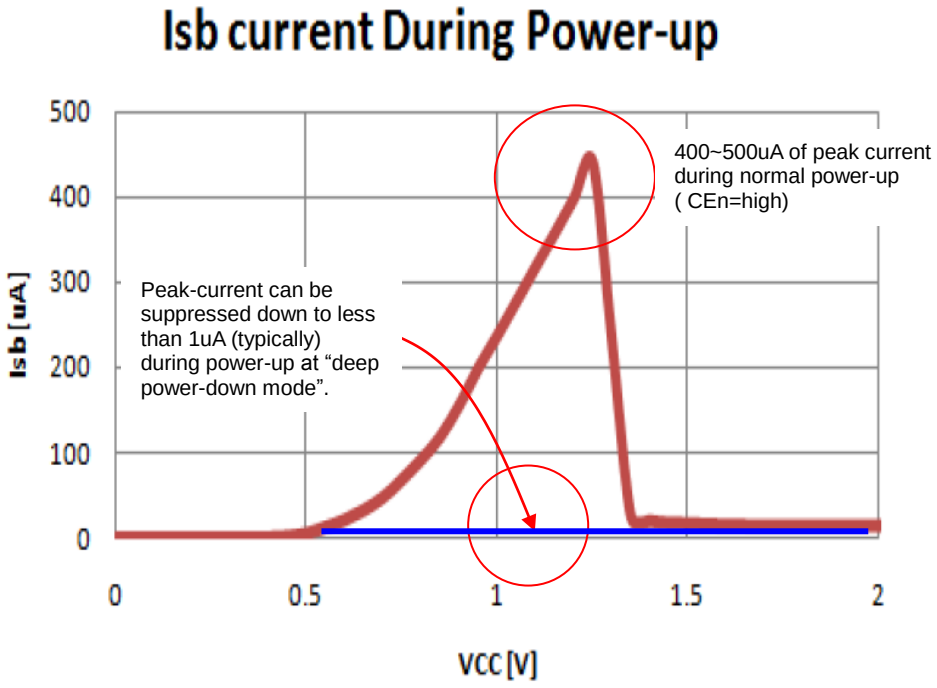
Table 14.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tXS	XUMn Setup Time	30			ns

13. Current during power-up

The device can enter the standby mode by applying a high signal to CEn input. Typically 20uA of current is consumed in the standby mode. But, during power-up, about **400uA** of peak current can flow when VCC rises to a stabilized level. This “peak current during power-up” can be suppressed down to **1uA** (typically) by keeping **PDOWNn** at Low during power-up.

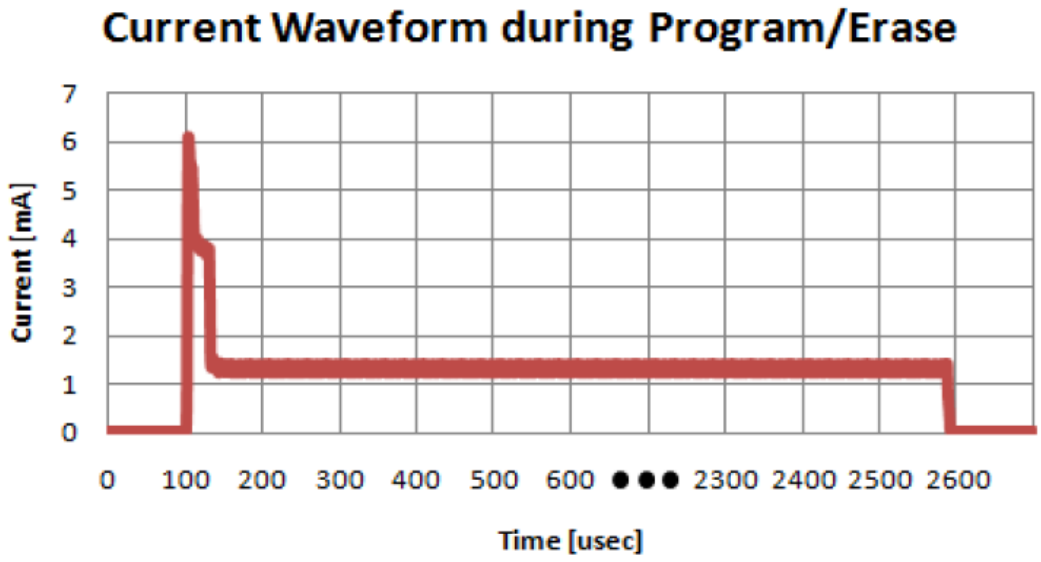
Fig. 10 Peak current during power-up at Stand-by mode



14. Peak current during write operation

At maximum, 8mA of peak current can flow at an initial stage of write operation. This is caused by initially activating charge pump circuit to generate high voltages for cell array into which data will be written. However, this peak-current is rapidly suppressed down to less than 1.5mA as soon as the internal charge pump operation is stabilized.

Fig. 11 Peak current during write operation



15. Device Reset (RSTn)

Sometimes, the device needs to be reset or initialized.
All internal registers and latches including the **page buffer** are completely cleared by the device reset. When **RSTn** pin is driven to low, any in-progress operation is immediately terminated. When applying “device reset” during write operation (program or erase), the write operation will be immediately interrupted and terminated. Therefore, they (the interrupted operations) need to be reinitiated to ensure data integrity which may have been corrupted by immediate termination of the write process. The device gets ready for read immediately just after the device gets out of the device reset by driving RSTn from low to high.

Fig. 12 Reset

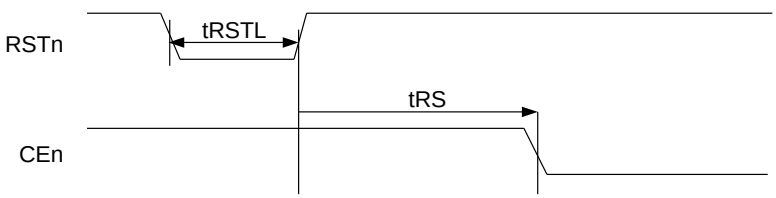


Table 15.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRSTL	RSTn Low Width Time	20			ns
tRS	RSTn Setup Time	100			ns

16. Deep power-down mode

In case that extremely small power consumption is required in stand-by mode, the deep power-down mode is recommended. In this mode, typically **less than 1uA** is consumed. By just asserting low to PDOWNn input, the device can be forced to enter the deep mode. In this mode, all circuits are completely turned off. At the same time, all internal registers and latches including the **page buffer** are reset to all “0”. Furthermore, any in-progress operation (such as write operation) is immediately terminated. However, **100usec of wake-up time** is required for the device to return to the normal read mode after the device gets out of this deep power-down mode.

Fig. 13 Deep power-down mode

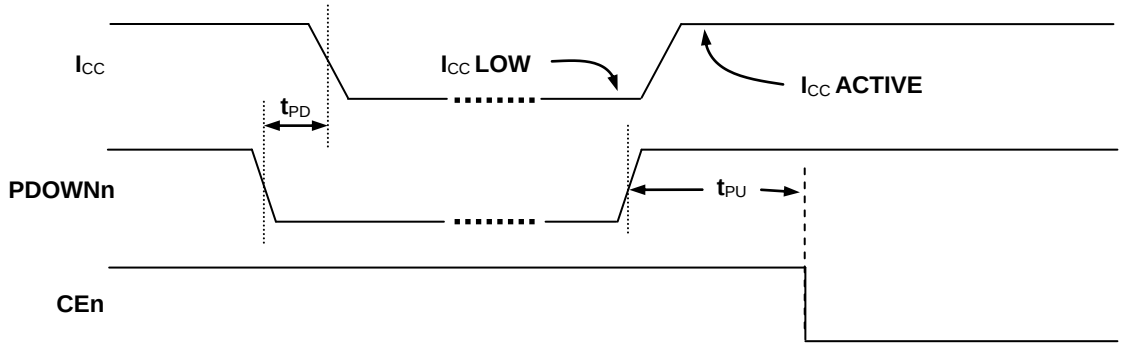


Table 16.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tPD	Power Down Time			5	us
tPU	Power Up Time	100			us

17. Power-up with PDOWNn (RSTn) signal

During power-up, all circuit environments get unstable, including the internal band-gap circuit.
So, PDOWNn or RSTn signal should be kept low until the power is fully raised and finally stabilized as shown in the figure 14.

Fig. 14 Power-up Sequence with PDOWN (RSTn) signal

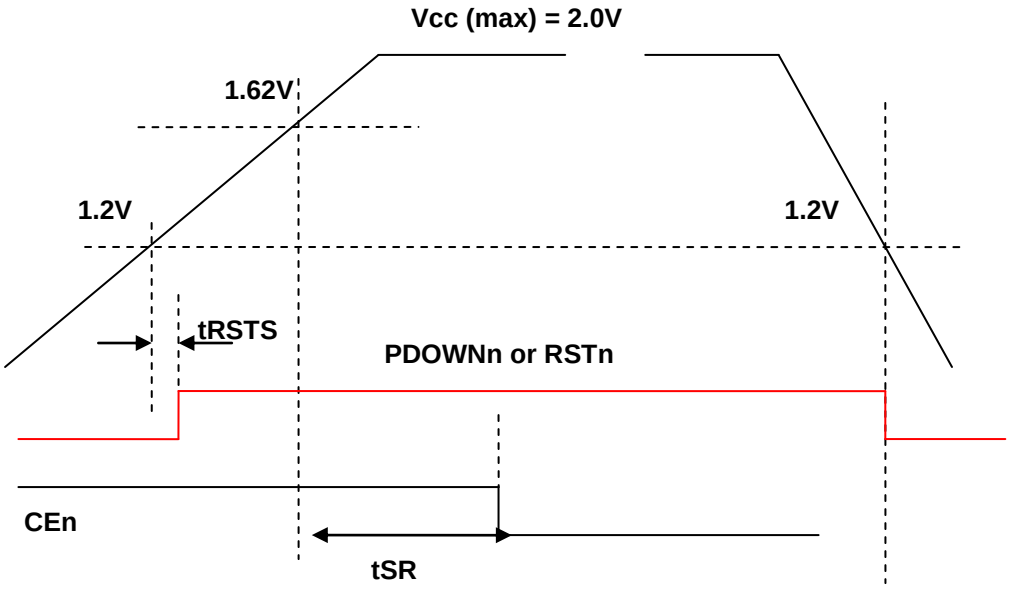


Table 17.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRSTS	PDOWNn (or RSTn) Set Time	0			ns
tSR	System Ready during power up	100			us

18. DC Operating Characteristics

Table 18.

Description	Symbol	Condition		Min	Typ	Max	Unit
Operation Temperature	Temp.	Read		-40	25	85	℃
		Write		-20	25	85	℃
Power Supply Voltage	V_{DD}			1.62	1.8	1.98	V
Stand By Current	I_{SB}	CEn= High	G		20	100	μA
			W		20	50	μA
Power Down Current	I_{PD}	PDOWNn= Low	G		1	80	μA
			W		1	30	μ
Read Current (Output Disabled by OEn=High)	I_{CC}	1MHz			2	4	mA
		10MHz			4	8	mA
Write Current	I_{WR}	Byte or page Write			1.5	8	mA
Input Low Voltage	V_{IL}			-0.3	0	0.1	V
Input High Voltage	V_{IH}			V_{DD} -0.3	V_{DD}	V_{DD} +0.3	V
Output High Voltage	V_{OH}	Ioh=1uA		V_{DD} -0.1		$0.9XV_{DD}$	V
Output Low Voltage	V_{OL}	Iol=1uA		-0.3		$0.1XV_{DD}$	V
Input Capacitance	C_{IN}	V_{IL}=0V; Temp. =25℃				0.1	pF
Output Capacitance	C_{OUT}	V_{IL}=0V; Temp. =25℃				0.1	pF

(Note) G (WC18EH3CG), W (WC18EH3CW)

Revisions

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Note

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